AMENDMENTS TO THE CLAIMS

Listing Of Claims

Claims 1-33 (Canceled)

34. (currently amended) A method for fabricating an interconnect for electrically engaging ~~a bumped contact on~~ a semiconductor component having at least one bumped contact comprising:

providing a substrate having a surface;

forming a plurality of leads on the surface configured to electrically engage and support the bumped contact, the leads having terminal portions and support portions;

~~etching~~ forming a recess in the surface configured to cantilever the terminal portions over the recess with the support portions on the surface supporting the terminal portions for movement within the recess during electrical engagement of the bumped contact, the recess sized and shaped to retain and center the bumped contact during the electrical engagement, the recess having a diameter approximately equal to that of the bumped contact and a depth approximately equal to a height of the bumped contact.

35. (previously presented) The method of claim 34 further comprising forming outer layers on the terminal portions configured to provide a non bonding surface for the bumped contact.

36. (withdrawn) The method of claim 34 wherein forming the plurality of leads comprises attaching a polymer tape to the substrate with the leads formed thereon.

37. (withdrawn) The method of claim 34 wherein forming the plurality of leads comprises etching beams in the substrate within the recess and covering the beams with conductive layers.

38. (currently amended) The method of claim 34 wherein the substrate comprises a semiconductor material, ~~and~~ the ~~etching~~ forming the recess step comprises anisotropic etching, and the recess has straight sidewalls sloped at an angle of about 55° with respect to the surface.

39. (currently amended) A method for fabricating an interconnect for electrically engaging ~~a bumped contact on~~ a semiconductor component having at least one bumped contact comprising:

providing a substrate having a surface;

~~forming a metal layer on the surface;~~

~~etching a plurality of projections in the metal layer configured to penetrate the bumped contact;~~

~~forming an outer layer on the metal layer configured to provide a non-bonding surface for the bumped contact;~~

forming a plurality of leads ~~in the metal layer~~ on the substrate configured to electrically engage and support the bumped contact, the leads having terminal portions with the projections thereon and support portions; and

etching a recess in the surface configured to cantilever the terminal portions over the recess with the support portions on the surface supporting the terminal portions for movement within the recess during electrical engagement of the bumped contact, the recess having shaped sidewalls configured to retain and center the bumped contact during the electrical engagement.

40. (currently amended) The method of claim 39 wherein the etching step comprises anisotropic etching and

the sidewalls are sloped at an angle with respect to the surface.

~~outer layer comprises a conductive polymer.~~

41. (currently amended) The method of claim 39 wherein the etching step comprises isotropic etching and the sidewalls are curved.

~~outer layer comprises a material selected from the group consisting of a carbon film and a metal filled silicone.~~

42. (withdrawn) The method of claim 39 further comprising shaping the leads with a radius of curvature corresponding to a diameter of the bumped contact.

43. (previously presented) The method of claim 39 further comprising forming a connecting segment on the substrate electrically connecting the leads, a conductive via in the substrate in electrical communication with the connecting segment and a contact on the substrate in electrical communication with the conductive via.

44. (withdrawn) A method for fabricating an interconnect for testing a semiconductor component comprising:

providing a substrate;

forming a recess in the substrate;

providing a tape comprising a polymer substrate comprising an opening therein and a plurality of leads on the substrate cantilevered over the opening;

aligning the leads with the recess; and

attaching the tape to the substrate with the leads cantilevered over the recess to form a contact for electrically engaging a bumped contact on the component.

45. (withdrawn) The method of claim 44 further comprising providing the tape with an electrical connector configured for electrical connection to test circuitry.

46. (withdrawn) A method for fabricating an interconnect for testing a semiconductor component comprising:

providing a substrate;

etching a recess in the substrate sized and shaped to retain a bumped contact on the component;

etching a plurality of beams within the recess configured to move within the recess and to support the bumped contact within the recess;

etching a plurality of projections on the conductive beams configured to penetrate the bumped contact; and

forming a conductive layer on the beams and the projections to form a contact for electrically engaging the bumped contact.

47. (withdrawn) The method of claim 46 further comprising controlling the etching of the beams step to form the beams with a cantilever length, a width, and a thickness selected to provide a desired spring constant.

48. (withdrawn) The method of claim 46 wherein the substrate comprises silicon and further comprising forming an electrically insulating layer on the beams prior to forming the conductive layer.

49. (currently amended) A method for fabricating an interconnect for electrically engaging ~~bumped contacts on~~ a semiconductor component having a plurality of bumped contacts comprising:

providing a substrate;

forming a plurality of interconnect contacts on the substrate configured ~~for~~ to electrically engage ~~ment of~~ the

bumped contacts, each interconnect contact comprising a plurality of leads having terminal portions and projections on the terminal portions;

~~etching~~ forming a plurality of recesses in the substrate proximate to the leads configured to cantilever the terminal portions of the leads for movement within the recesses during the electrical engagement, the recesses configured to retain and center the bumped contacts during the electrical engagement, each recess having a diameter approximately equal to that of a bumped contact and a depth approximately equal to or less than a height of the bumped contact; and

forming outer layers on the terminal portions and projections configured to provide non-bonding surfaces for the bumped contacts.

50. (previously presented) The method of claim 49 wherein the outer layers comprise a conductive polymer.

51. (previously presented) The method of claim 49 wherein the projections comprise blades.

52. (withdrawn) The method of claim 49 wherein the forming the conductive vias step comprises laser machining.

53. (withdrawn) A method for fabricating an interconnect for a semiconductor component having a bumped contact comprising:

providing a substrate having a surface and an opposing surface;

forming a plurality of leads on the surface configured to electrically engage the bumped contact;

forming a connecting segment on the surface electrically connecting the leads;

forming a recess in the surface with the leads cantilevered over the recess and configured to support the bumped contact for movement within the recess;

shaping the leads with a radius of curvature corresponding to a diameter of the bumped contact;

forming a conductive via in the substrate in electrical communication with the connecting segment; and

forming a contact on the opposing surface in electrical communication with the bumped contacts.

54. (withdrawn) The method of claim 53 further comprising forming a plurality of blades on the leads configured to penetrate the bumped contact.

55. (withdrawn) The method of claim 53 wherein the forming the conductive via step comprises laser machining an opening through the connecting segment and the substrate.

56. (withdrawn) The method of claim 53 wherein the contact comprises a pad.

57. (withdrawn) The method of claim 53 wherein the forming the conductive via step comprises electrically insulating and then at least partially filling an opening with a conductive material.

58. (withdrawn) The method of claim 53 wherein the substrate comprises a material selected from the group consisting of silicon, ceramic and plastic.